# Reference-less, real time on-chip Clock Jitter measurement IP

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# Agenda



- Motivation
- Impact of clock Jitter on a Delta Sigma Modulator
- Novel Jitter measurement architecture
- Simulation results
- Key Benefits
- Applications
- Conclusion

# Motivation

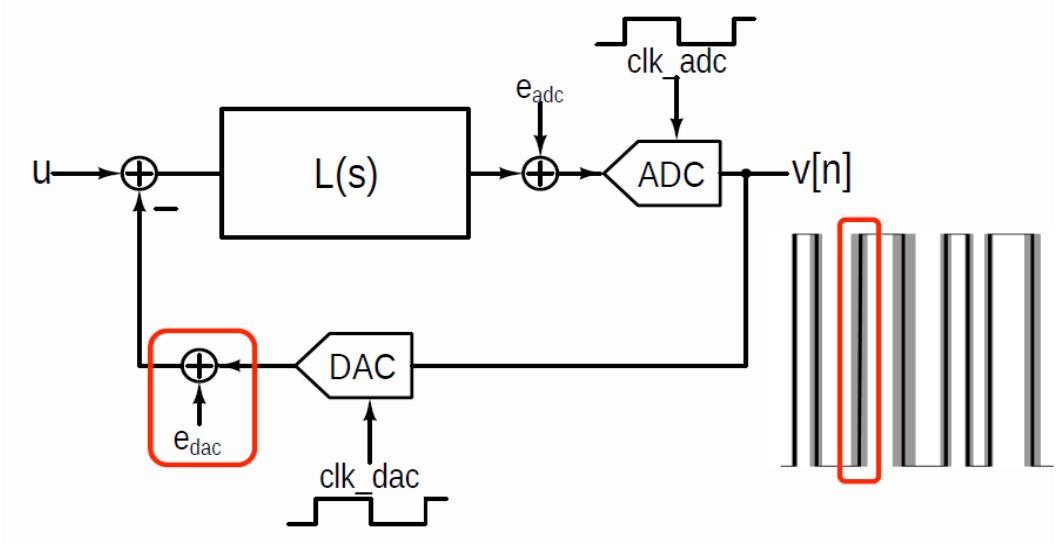


- In high-speed ASICs, clock jitter is one of the most critical parameters that can affect system performance.
- To achieve high design reliability, jitter measurement is becoming indispensable
- Off chip measurement methods (using ext. jitter equipment like spectrum analyzer etc.) are irrelevant for High speed ASICs production tests.
- Conventional on-chip jitter measurement need jitter free clean reference clock.
- Also very accurate and constant delay components in nanometer technologies are very difficult as their properties vary with PVT

# Impact of Clock Jitter on a Delta Sigma Modulator



Jittery clock → equivalent to error at the input




- Additive error following the DAC => *e*2(*t*) depends on DAC properties.
- Equivalent to adding an error at the modulator input.
- Degrades performance. Merits careful analysis.

# Effect of Clock Jitter on NRZ DACs

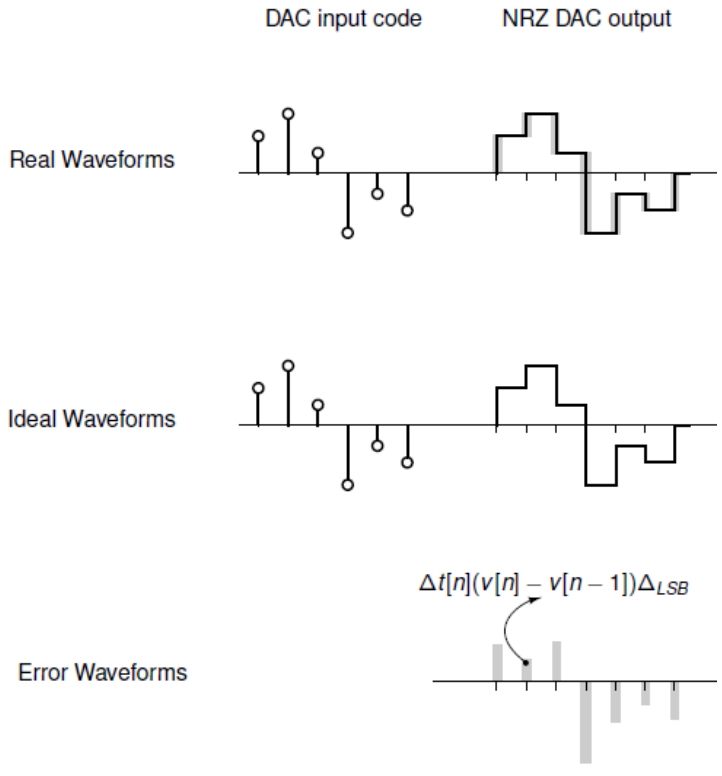


$$\varepsilon(n) = (y(n) - y(n-1))\frac{\Delta T(n)}{T_s}$$

The in-band Signal to noise ratio due to jitter

$$SNR_j = \frac{A^2/2}{B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2\omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3}\right]}$$

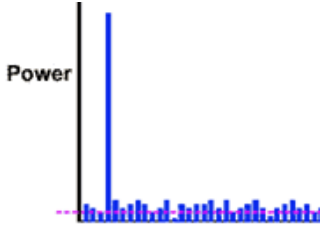
A - signal amplitude, $\omega_i$ - angular freq. $B_w$ - bandwidth
and $\sigma_{\Delta T}$ is clock jitter standard deviation of the modulator clock

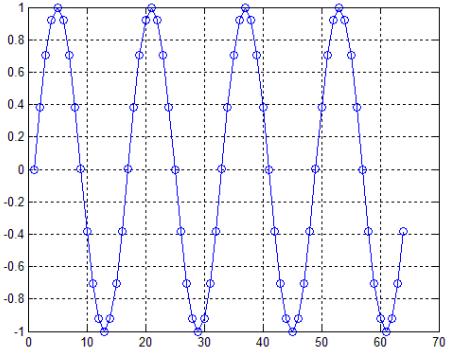


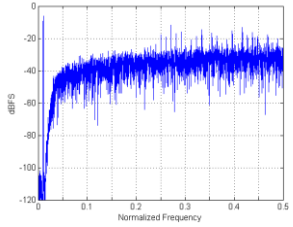

Ref: “Effect of Clock Jitter Error on the Performance degradation of Multi-bit Continuous-Time ΣΔ Modulators With NRZ DAC”, TEC2004-01752/MIC January 2005.

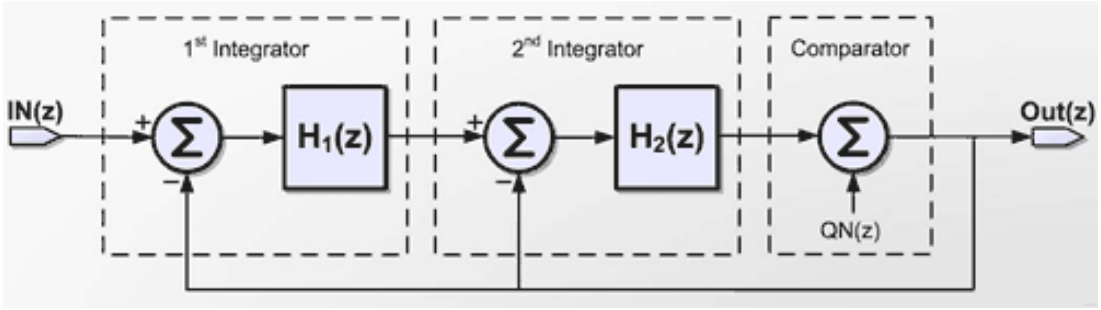
# Test Signal Generation

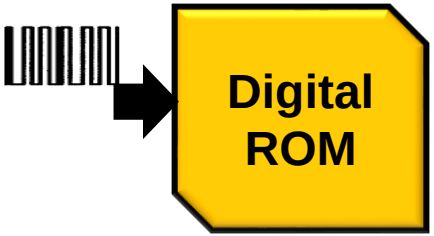







**Digital Higher Order Modulator**

$$X_k = \sum_{n=0}^{N-1} x_n \cdot e^{-\frac{2\pi i}{N} kn}$$

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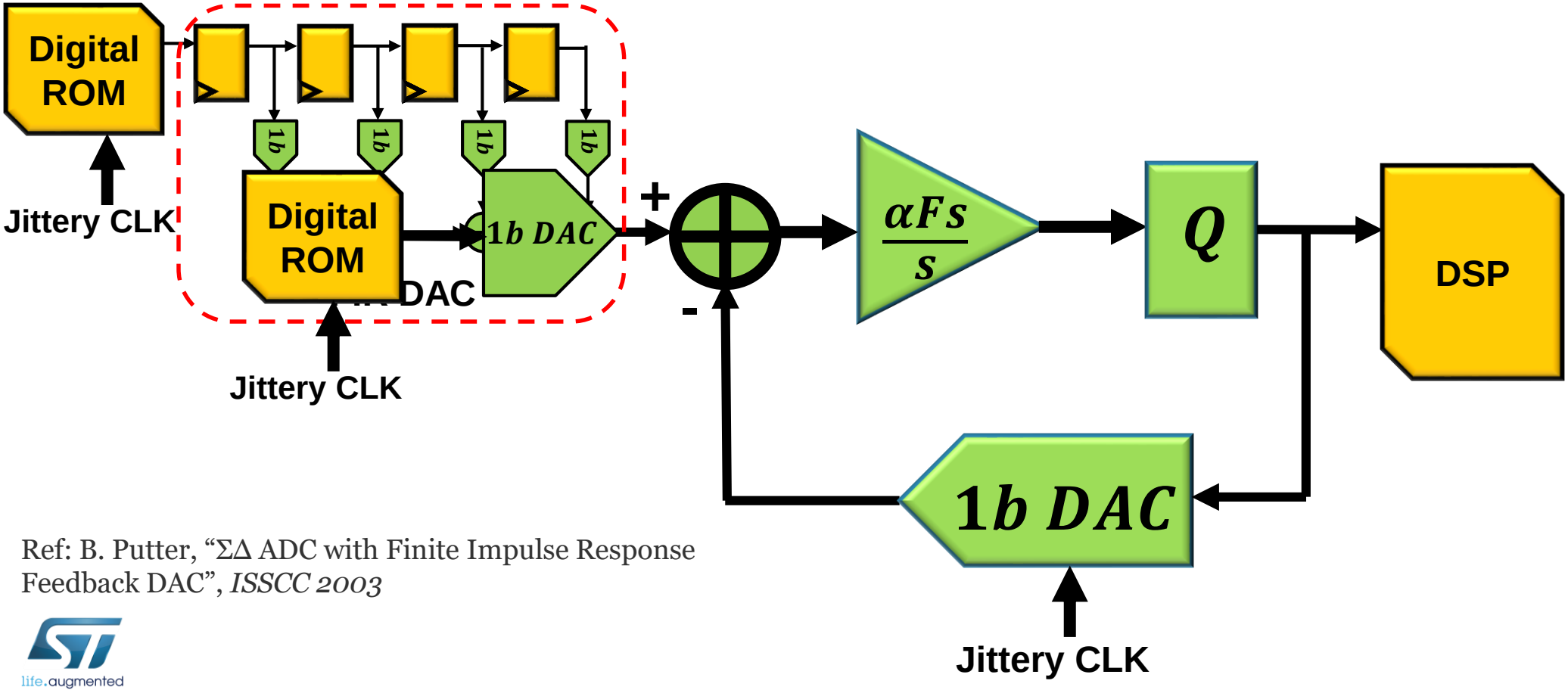
# Novel Jitter measurement IP

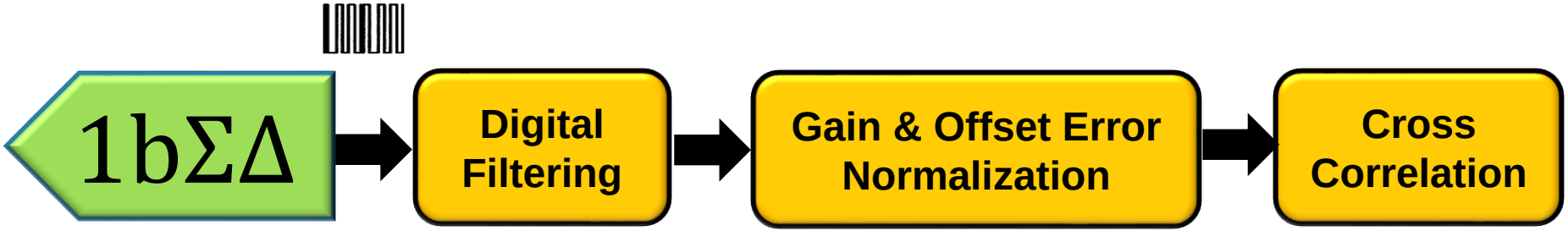


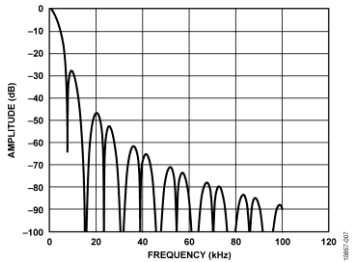



Ref: B. Putter, "ΣΔ ADC with Finite Impulse Response Feedback DAC", *ISSCC 2003*

# Response Analyses






$$Amp = 2 \cdot \frac{1}{563} \cdot \frac{1}{Amp_{REF}} \cdot \sum_{i=1}^{563} S_{out}[i] \cdot S_{ref}[i]$$

$$S_{ref,fitted}[i] = Amp \cdot \frac{1}{Amp_{REF}} \cdot S_{ref}[i] + DC$$

$$P_{error} = \frac{\sum_{i=1}^{563} \left(S_{out}[i] - S_{ref,\,fitted}[i]\right)^2}{563}$$

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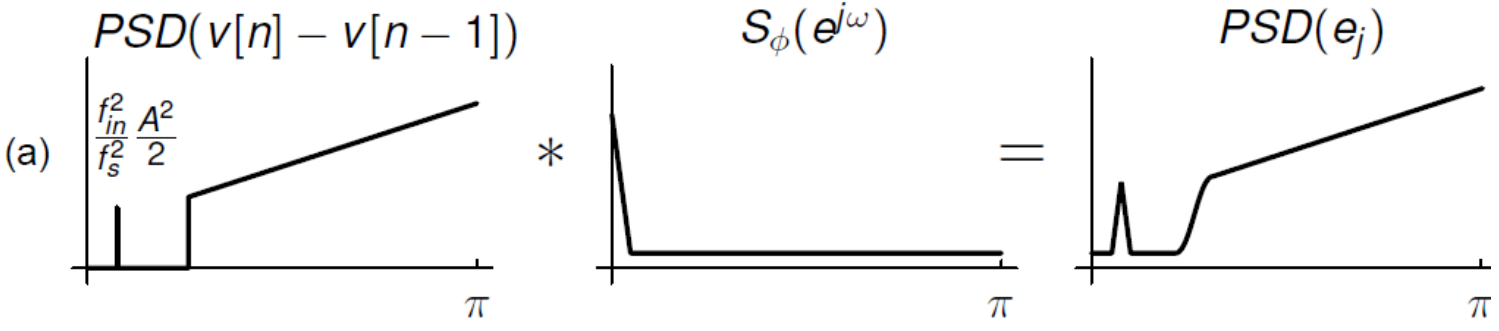
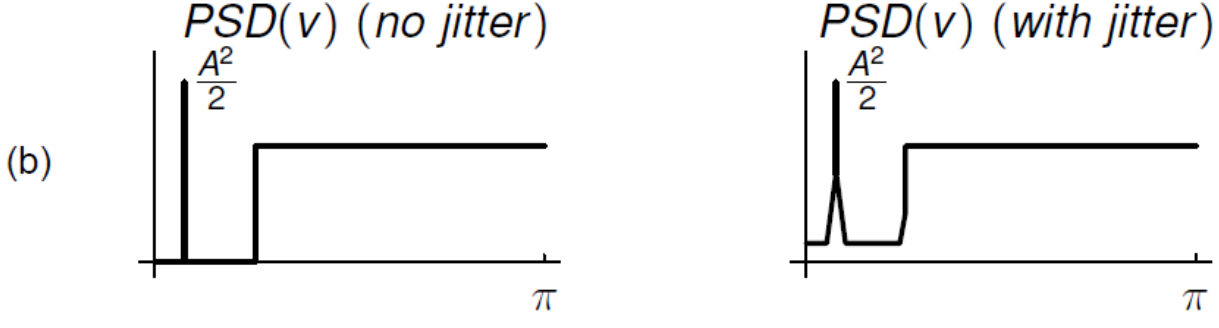
Ref: A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40 nm CMOS 18-bit Stereo Audio CTSD-ADC, *IEEE Transactions on Circuits and Systems I*, Oct. 2016

# Real Clocks and Phase Noise



$$e_j[n] = (v[n] - v[n-1])(\Delta t[n]/T_s)$$

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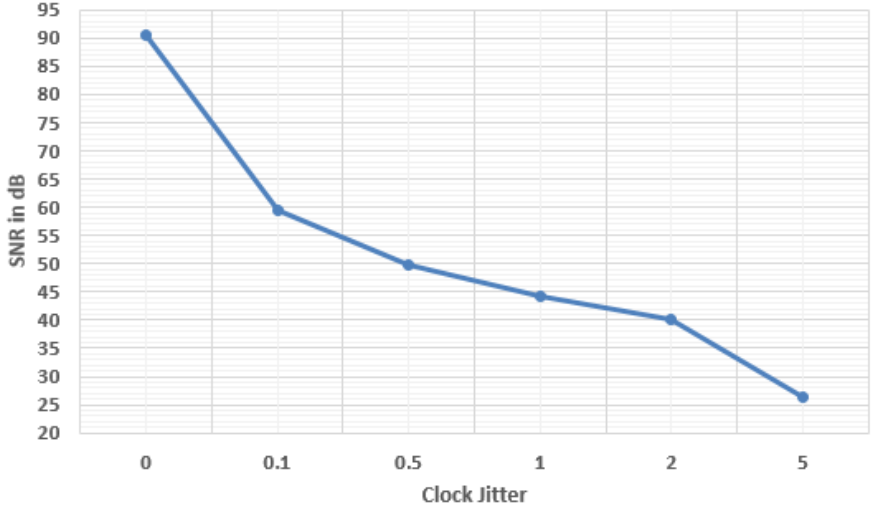
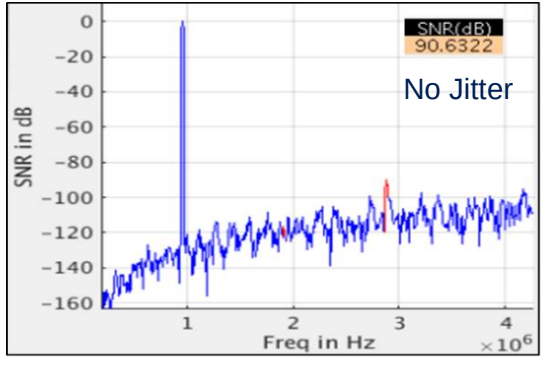
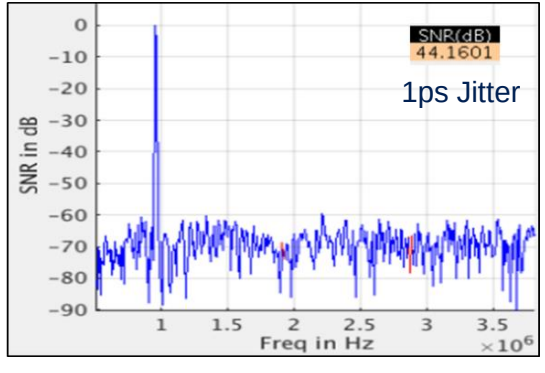
# Simulation Results



## Influence of clock jitter on a continuous time (CT) sigma-delta ADC




- Illustration of in band frequency spectrum with the system clock subject to jitter degradation.
- High measurement resolution less than 1pS is achieved.

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# Key Benefits



- Fully on chip solution
- Obviates need of any reference clock or PLL
- Can help SoC architect as a jitter sensor and thus reduce design margins (SoC PPA improvement)
- High resolution quantification of rms jitter
- Immune to PVT variations
- Multi probe solution leads to low area overhead

# Applications

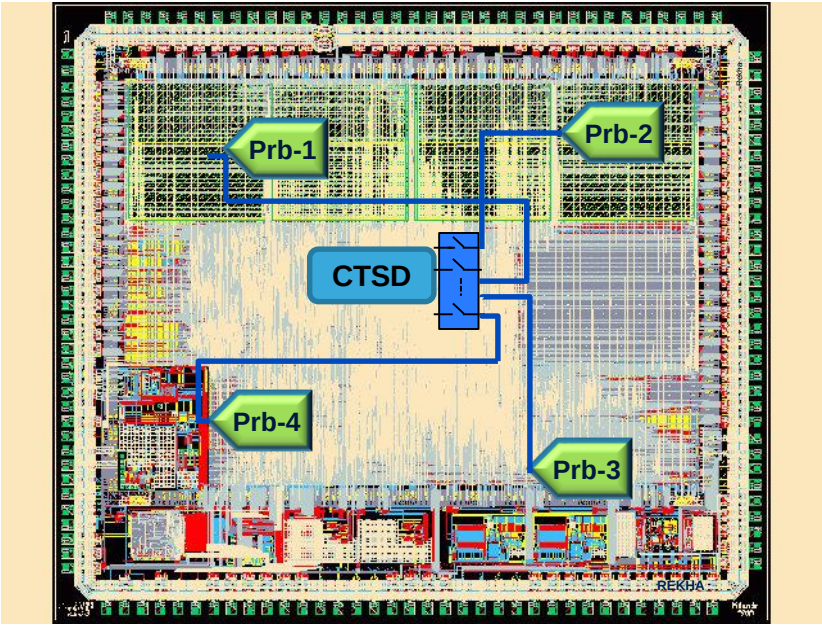


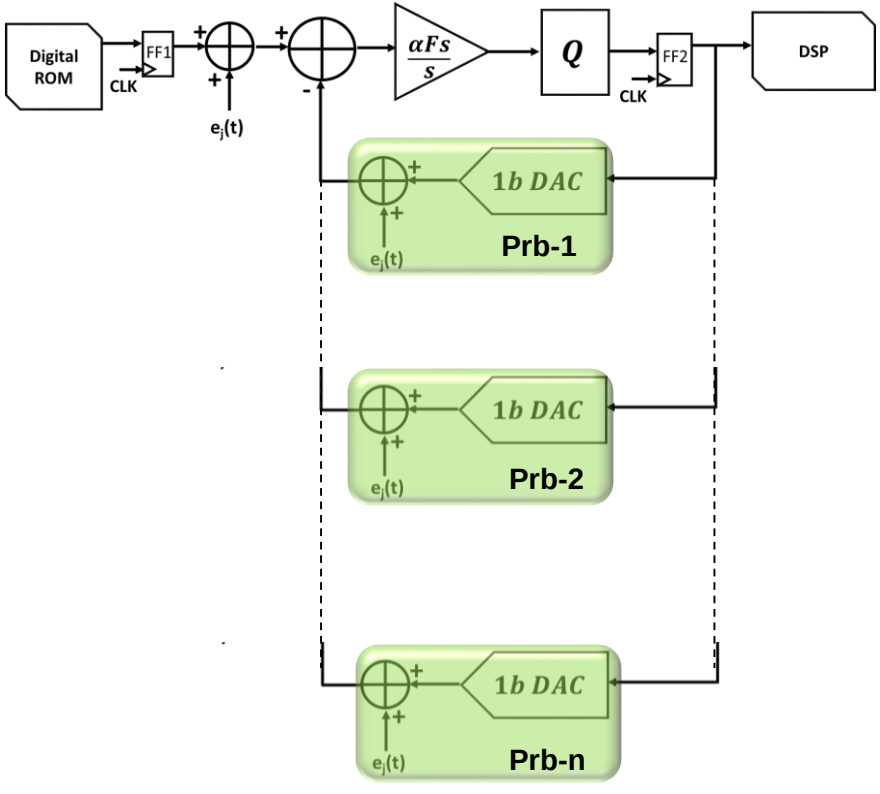
- PLL BIST
- On-chip real time BER qualifier in production
- High speed jitter monitoring probe in CPUs/GPUs
- Jitter analyzer in communication SoCs
- Dedicated jitter analyzer chip for PCB production tests

# Round Robin Probing



## Remote probes across chip



# Conclusion



- CTSD-ADC performance degradation can be used to accurately quantify clock jitter with very high precision.
- A Single bit, two level quantizer has maximum jitter sensitivity
- Phase Noise can also be quantified
- Test out multiple methods for initial modulator calibration
- Owing to the CTSD modulator overhead, a multiple probe system can be used to measure jitter across the device
- This approach can be extended to board level measurements